



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,083	04/19/2001	Woo Sik Yoo	M-11439 US	9578

7590 09/09/2003
Theodore P. Lopez
MacPherson Kwok Chen & Heid LLP
2402 Michelson Drive
Suite 210
Irvin, CA 92612

EXAMINER

FOX, CHARLES A

ART UNIT PAPER NUMBER

3652

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Caveney et al. In regards to claim 11 Caveney et al. US 5,765,983 discloses a system for transporting semiconductor wafers comprising:

a process system including a process chamber (26) and a transport module (22);

a wafer transport device (24) disposed in said transport module (22);

a container (42) configured to hold a plurality of wafers;

said container being and remaining a separate component from said processing system;

wherein said wafer transport device is designed to extend into said container and remove a wafer for delivery to a process chamber;

wherein said transport device (24) is exposed to the ambient environment.

In regards to claim 12 Caveney et al. also disclose that said wafer transport device comprises a robot with an extensible arm and an end effector.

In regards to claim 13 Caveney et al. further disclose that the wafer transport device is fixed within the transport chamber.

In regards to claim 18 Caveney et al. also discloses a gate valve assembly between the transport module and the process chamber.

In regards to claim 19 Caveney et al. disclose that the wafer container is a cassette.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caveney et al. in view of Gordon et al. In regards to claims 1 and 14 Caveney et al. teach a method of transporting semiconductor wafers comprising the steps of:

providing a processing system including a transport module and a process chamber;

extending a transport robot into a cassette while said cassette remains a distinct component from said system;

exposing the wafer transport robot to the ambient environment;

removing at least one wafer from said cassette;

placing said removed wafer into a process chamber via an extendable arm on said robot.

Caveney et al. do not teach the cassette as being a FOUP device. Gordon et al. US 6,013,920 teaches a method of handling wafers from a FOUP. It would have been obvious to one of ordinary skill in the art, at the time of invention to modify the methods taught by Caveney et al. by providing the cassette as a FOUP as taught by Gordon et al. in order to allow the device to operate using cassettes that maintain the wafers in a clean state as they are moved about the process area.

In regards to claim 2 Caveney et al. also teach that said wafer transport device comprises a robot with an extensible arm and an end effector.

In regards to claim 3 Caveney et al. further teach that the wafer transport device is fixed within the transport chamber.

In regards to claim 9 Caveney et al. also teaches opening a gate valve assembly between the transport module and the cassette to allow said transport device to extend into said cassette.

Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caveney et al. in view of Gordon et al. as applied to claim 1 above, and further in view of Beaulieu et al. (US 5,882,413). Caveney et al. in view of Gordon et al. teach the limitation of claim 1 as above they do not teach using a storage location or the type of processing chamber used or the use of a cooling chamber. Beaulieu et al. (US 5,882,413) disclose a method for transporting semiconductor wafers comprising:

providing a processing system (10) including a transport module (12) and a process chamber (14);

extending a semiconductor transport device (22) from said transport module (12) into adjacently positioned container, said container being a separate component from said processing system;

removing at least one wafer (s) from said container using said wafer transporting device;

wherein the transport device (22) comprises a robot including an extendible arm and an end effector (29);

and the transport device (22) is in a fixed position;

placing the wafers (s) in a storage position (34);

wherein the process chamber is a chemical vapor deposition chamber;

transporting the wafers (s) between a cooling chamber (36) and a process chamber (14).

providing a processing system (10) including a transport module (12) and a process chamber (14);

extending a semiconductor transport device (22) from said transport module (12) into adjacently positioned container, said container being a separate component from said processing system;

removing at least one wafer (s) from said container using said wafer transporting device;

wherein the transport device (22) comprises a robot including an extendible arm and an end effector (29);

and the transport device (22) is in a fixed position;

placing the wafers (s) in a storage position (34);
wherein the process chamber is a chemical vapor deposition chamber;
transporting the wafers (s) between a cooling chamber (36) and a process chamber (14).

It would have been obvious to one of ordinary skill in the art, at the time of invention to modify the methods taught by Caveney et al. in view of Gordon et al. by moving the wafers into chambers and modules of various sorts are taught by Beaulieu et al. and are well known in the art.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Caveney et al. in view of Gordon et al. as applied to claim 1 above, and further in view of Moore et al. Caveney et al. in view of Gordon et al. teach the limitations of claim 1 as above, they do not teach the processing system as comprising a single rapid thermal processing chamber. Moore et al. (US 6,151,447) teach an apparatus with a rapid thermal processing chamber. It would have been obvious to one of ordinary skill in the art, at the time of invention that a rapid thermal chamber as taught by Moore et al. could have been used as the process chamber taught by Caveney et al. in view of Gordon et al. as modular chambers are well know in the art, and said chambers are designed to perform many processing steps including rapid thermal processing.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caveney et al. as applied to claim 11 above, and further in view of Beaulieu et al. Caveney et al. teach the limitations of claim 11 as above they do not teach the system

Art Unit: 3652

having a storage location or the type of processing chamber used or a cooling chamber.

Beaulieu et al. disclose an apparatus for transporting semiconductor wafers comprising:

a processing system (10) including a transport module (12) and a process chamber (14);

an extending semiconductor transport device (22) ;

wherein the transport device (22) comprises a robot including an extendible arm and an end effector (29);

and the transport device (22) is in a fixed position;

a storage position (34);

wherein the process chamber is a chemical vapor deposition chamber;

a cooling chamber (36) and a process chamber (14);

It would have been obvious to one of ordinary skill in the art, at the time of invention to modify the device taught by Caveney et al. in view of Gordon et al. by providing the chambers and modules of various sorts are taught by Beaulieu et al. as they are well known in the art.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Caveney et al. as applied to claim 11 above, and further in view of Moore et al. Caveney et al. teach the limitations of claim 11 as above, they do not teach the processing system as comprising a single rapid thermal processing chamber. Moore et al. teach an apparatus with a rapid thermal processing chamber. It would have been obvious to one of ordinary skill in the art, at the time of invention that a rapid thermal chamber as taught by Moore et al. could have been used as the process chamber taught by Caveney et al.

as modular chambers are well know in the art, and said chambers are designed to perform many processing steps including rapid thermal processing.

Response to Amendment

The amendments to the claims filed on June 18, 2003 have been entered into the record.

Response to Arguments

Applicant's arguments filed June 18, 2003 have been fully considered but they are not persuasive. In regards to the arguments against the combination of the Caveney et al. and Gordon et al. references, the Gordon et al. reference is used as a reference citing the use of FOUP containers to transport wafers in a manufacturing setting. Gordon is used only as teaching the use of FOUP'S and not for any other structure as applied to claim 1. Therefore Gordon et al. teach using the FOUP as opposed to a generic cassette taught by Caveney et al who teach all other limitations of the claim.

In regards to the arguments against claim 11 Caveney et al. do teach the transport robot exiting the transport load lock into the ambient atmosphere to place or remove a wafer into or from the cassette that is open to the ambient atmosphere. In fact the cassette is situated very much like the FOUP illustrated in figure 2A of the instant invention.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A. Fox whose telephone number is 703-605-4294. The examiner can normally be reached between 7:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eileen D. Lillis can be reached at 703-308-3248. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1113.

CAF
CAF
8-24-03


EILEEN D. LILLIS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600